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EXAMINER	
WILLIAMS, LAWRENCE B	

ART UNIT	PAPER NUMBER
2634	

DATE MAILED: 03/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/531,677	BABA, HIROSHI	
	Examiner	Art Unit	
	Lawrence B Williams	2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *RCE filed on 14 April 2004* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 March 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *2* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Objections

1. Claim 11 is objected to because of the following informalities: Examiner suggests applicant rephrase lines 9-10 of the claim for clarification purposes.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

3. Claim 11 recites the limitation "the reference frequency divided signal" in line 4. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-11 are rejected under 35 U.S.C. 102(e) as being anticipated by Jokura (US Patent 6,173,025 B1).

(1) With regard to claim 1, Jokura discloses in Fig. 1, a method of controlling a power saving operation for a phase comparator unit, comprising the steps of: dividing (9) a frequency of a reference signal (Freq. Ctrl) to generate a reference frequency divided signal; dividing (3) a frequency of an input signal (1) to generate a comparison frequency divided signal a phase of which is to be compared with a phase of the reference frequency divided signal; comparing (4) the phases of the reference frequency divided signal and the comparison frequency divided signal so as to output a comparison result; generating a power saving state canceling signal (SW) in accordance with the reference frequency divided signal and the comparison frequency divided signal; generating a first initializing signal for initializing the output of the step of dividing the frequency of the reference signal in accordance with the power saving state canceling signal (signal from Control to Gate); and generating a second initializing signal (signal from Control to Gate) for initializing the output of the step of dividing the frequency of the input signal in accordance with the power saving state canceling signal (col. 1, line 36 - col. 2, lines 7).

(2) With regard to claim 2, Jokura also discloses wherein frequency dividing rates used in the step of dividing the frequency of the reference signal and in the step of dividing the frequency of the input signal can be set independently of each other (col. 1, lines 45-48).

(3) With regard to claim 3, Jokura discloses in Fig(s). 1, a power saving operation control circuit for a phase comparator unit, comprising; a reference signal frequency dividing unit (9) which divides a frequency of a reference signal (Freq. Ctrl) to generate a reference frequency divided signal; a comparison signal dividing unit (3) which divides a frequency of an input signal (1) to generate a comparison frequency divided signal whose phase is to be compared with a phase of the reference frequency divided signal; a phase comparator (4) which compares the

phases of the reference frequency divided signal and the comparison frequency divided signal so as to output a comparison result; a cancel signal generator (10) which generates a power saving state canceling signal in accordance with the reference frequency divided signal and the comparison frequency divided signal; a first initializing signal generator (8) which generates a first initializing signal for initializing the reference signal frequency dividing unit in accordance with the power saving state canceling signal; and a second initializing signal generator (2) which generates a first initializing signal for initializing the reference signal frequency dividing unit in accordance with the power saving state canceling signal (col. 1, line 36 - col. 2, lines 7).

(4) With regard to claim 4, Jokura also discloses wherein frequency dividing used rates used in the reference signal frequency dividing unit and in the comparison signal frequency dividing unit can be set independently of each other (col. 1, lines 45-48).

(5) With regard to claim 5, Jokura also discloses in Fig. 1, a PLL frequency synthesizer comprising; a phase comparator unit (4); a loop filter (6) which receives an output of the phase comparator unit; and a voltage control oscillator (7) which receives an output of the loop filter, the phase comparator unit comprising: a reference signal frequency dividing unit (9) which divides a frequency of a reference signal to generate a reference frequency divided signal; a comparison signal dividing unit (3) which divides a frequency of an output signal of the voltage control oscillator to generate a comparison frequency divided signal a phase of which is to be compared with a phase of the reference frequency divided signal; a phase comparator (4) which compares the phases of the reference frequency divided signal and the comparison frequency divided signal so as to output a comparison result; a canceling signal generator (10) which generates a power saving state canceling signal in accordance with the reference frequency

divided signal and the comparison frequency divided signal; a first initializing signal generator (8) which generates a first initializing signal for initializing the reference signal frequency dividing unit in accordance with the power saving state canceling signal; and a second initializing signal generator (2) which generates a second initializing signal for initializing the comparison signal frequency dividing unit in accordance with the power saving state canceling signal.

(6) With regard to claim 6, claim 6 inherits all limitations of claim 5 above. Furthermore, Jokura also discloses wherein frequency dividing rates used in the reference signal frequency dividing unit and in the comparison signal frequency dividing unit can be set independently of each other (col. 1, lines 45-48).

(7) With regard to claim 7, Jokura also discloses in Fig. 1, a semiconductor integrated circuit including a PLL frequency synthesizer comprising: a phase comparator unit (4); a loop filter (6) which receives an output of the phase comparator unit; a voltage control oscillator (7) which receives an output of the loop filter, the phase comparator unit comprising: a reference signal frequency dividing unit (9) which divides a frequency of a reference signal to generate a reference frequency divided signal; a comparison signal dividing unit (3) which divides a frequency of an output signal of the voltage control oscillator to generate a comparison frequency divided signal a phase of which is to be compared with a phase of the reference frequency divided signal; a phase comparator (4) which compares the phases of the reference frequency divided signal and the comparison frequency divided signal so as to output a comparison result; a canceling signal generator (10) which generates a power saving state canceling signal in accordance with the reference frequency divided signal and the comparison

frequency divided signal; a first initializing signal generator (8) which generates a first initializing signal for initializing the reference signal frequency dividing unit in accordance with the power saving state canceling signal; and a second initializing signal generator (2) which generates a second initializing signal for initializing the comparison signal frequency dividing unit in accordance with the power saving state canceling signal.

(8) With regard to claim 8, claim inherits all limitations of claim 7 above. Furthermore, Jokura also discloses wherein frequency dividing rates used in the reference signal frequency dividing unit and in the comparison signal frequency dividing unit can be set independently of each other (col. 1, lines 45-48).

(9) With regard to claim 9, Jokura also discloses in Fig. 1, a transmitter-receiver including a PLL frequency synthesizer comprising: a phase comparator unit (4); a loop filter (6) which receives an output of the phase comparator unit; a voltage control oscillator (7) which receives an output of the loop filter, the phase comparator unit comprising: a reference signal frequency dividing unit (9) which divides a frequency of a reference signal to generate a reference frequency divided signal; a comparison signal dividing unit (3) which divides a frequency of an output signal of the voltage control oscillator to generate a comparison frequency divided signal a phase of which is to be compared with a phase of the reference frequency divided signal; a phase comparator (4) which compares the phases of the reference frequency divided signal and the comparison frequency divided signal so as to output a comparison result; a canceling signal generator (10) which generates a power saving state canceling signal in accordance with the reference frequency divided signal and the comparison frequency divided signal; a first initializing signal generator (8) which generates a first

initializing signal for initializing the reference signal frequency dividing unit in accordance with the power saving state canceling signal; and a second initializing signal generator (2) which generates a second initializing signal for initializing the comparison signal frequency dividing unit in accordance with the power saving state canceling signal.

(10) With regard to claim 10, claim 10 inherits all limitations of claim 9 above. Furthermore, Jokura also discloses wherein frequency dividing rates used in the reference signal frequency dividing unit and in the comparison signal frequency dividing unit can be set independently of each other (col. 1, lines 45-48).

(11) With regard to claim 11, Aizaka discloses in Fig. 1, a method of controlling a power saving operation for a phase comparator unit, comprising the steps of: dividing a frequency (3) of an input signal (1) to generate a comparison divided signal, a phase of which is to be compared with a phase of a reference frequency divided signal; comparing the phase of the reference frequency divided signal and the comparison frequency divided signal (4) so as to output a comparison result; generating a power saving state canceling signal in accordance with the reference frequency divided signal and the comparison frequency divided signal (Control); generating a initializing signal for initializing the output of the step of dividing the frequency of the reference signal (8) or the frequency of the input signal (2) in accordance with the power saving state canceling signal.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. Fang discloses in U. S. Patent 5,548,250 Low Power Phase Lock Loop Clocking Circuit For Battery Powered Systems.

b. Hirose discloses in U. S. Patent 5,598,405 Time Division Multiple Access Time Division Duplex Type Receiver Transmitter-Receiver.

c. Nakamichi discloses in U. S. Patent 6,518,845 B2 PLL-Frequency Synthesizer Circuit.

d. Yonekawa et al. discloses in U.S. Patent 5,410,571 PLL Frequency Synthesizer Circuit.

e. Yahagi et al. discloses in U.S. Patent 5,389,899 Frequency Synthesizer Having Quick Frequency Pull In And Phase Lock-In.

f.) Borras et al. discloses in U.S. Patent 4,631,496 Battery Saving System For A Frequency Synthesizer.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lawrence B Williams whose telephone number is 571-272-3037. The examiner can normally be reached on Monday-Friday (8:00-5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on 571-272-3056. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Lawrence B. Williams

lbw
March 4, 2005

Amanda

AMANDA T. LE
PRIMARY EXAMINER